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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	K. KAKI et al.
Serial No.:	10/784,995
Filed:	February 25, 2004
Title:	SEMICONDUCTOR STORAGE APPARATUS IN WHICH DIFFERENT ERASE COMMANDS ARE SEQUENTIALLYSENT TO A PLURALTY OF NONVOLATILE SEMICONDUCTOR MEMORIES
Group:	2189
Examiner:	INOA, Midys
Confirmation No.:	9779

REQUEST FOR RECONSIDERATION

Mail Stop: AF **June 6, 2006**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

In response to the Final Office Action dated March 6, 2006, Applicants respectfully request reconsideration of the reasons set forth below.

In the Office Action, the rejection is based on the combination of USP 5,724,544 to Nishi and USP 6,826,113 to Ellis. In particular, the Office Action admits that Nishi lacks an important claimed element. More specifically, the Office Action states in the second paragraph on page 2 that:

> "Nishi does not teach these erase signals being interleaved or parallel to one another (as claimed, "initiating the second erase command while the first erase operations is still being performed ..."). "

However, the Office Action goes on to state "this limitation is taught by Ellis."